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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,019	12/07/2001	Francesco Pessolano	NL 000667	8972

24737 7590 06/15/2009
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
06/15/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/020,019	PESSOLANO ET AL.	
	Examiner	**Art Unit**	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13,14 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13,14 and 16-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-11, 13-14, and 16-24 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 4/9/2009.

Withdrawn objections and rejections

3. The claim objections for claims 5-8 and 10 have been withdrawn due to amendment.

4. The 35 U.S.C. 112 second paragraph rejections for claims 3 and 8 have been withdrawn due to amendment.

Claim objections

5. Claim 2 is objected to because of the following informalities:

6. Claim 2 recites “further comprising FIFO” that should be changed to “further comprising a FIFO.”

7. Appropriate correction is required.

Maintained Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 5-11, 13-14, and 16-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Masse et al. (U.S. 6,990,570), in view of Redford (U.S. 6,732,253).

10. As per claim 1:

Masse disclosed a digital signal processing apparatus for executing a plurality of operations, comprising:

a functional unit wherein the functional unit is adapted to execute operations (Masse: Figure 10 element 904, column 11 lines 13-18), and

control means for controlling the functional units (Masse: Figure 10 elements 918 and 932, column 10 lines 1-18 and column 11 lines 1-33) wherein control means includes:

a fetch unit, a decode unit (Masse: Figure 5 elements 204 and 206, column 6 lines 48-67 continued to column 7 lines 1-7)(The processor includes a fetch and decode stage in the processor pipeline.), and

a control units responsive to the decode unit (Masse: Figure 5 element 206, Figure 10 elements 918 and 932, column 10 lines 1-18 and column 11 lines 1-33)(Elements 918 and 932 make up the control unit that is coupled to the functional unit. The decode unit of figure 5 tells the control unit of figure 10 that the instruction is a repeat instruction, which causes it to be repeated according to the counter element.),

wherein each functional unit has a corresponding control unit for controlling a function of the functional unit defined by one or more operations from the decode unit,

including controlling a number of repetitions of execution of the function (Masse: Figure 5 element 206, Figure 10 elements 918, 922, and 932, column 11 lines 23-33)(Elements 922 and 932 control the number of repetitions of the repeat instruction. The ALU has its own private control unit in elements 918, 922, and 932. The decode unit of figure 5 tells the control unit of figure 10 that the instruction is a repeat instruction, which causes it to be repeated according to the counter element.), and

each functional unit is adapted to execute the operations for the number of repetitions in an autonomous manner under control of the control unit associated with the functional unit (Masse: Figure 10 elements 904, 918, 922, and 932, column 11 lines 1-33)(The control logic allows for the repeated execution of the repeat instruction according to the count value by the ALU.),

Masse failed to teach a plurality of functional units and a plurality of control units.

However, Redford disclosed a plurality of functional units and a plurality of control units (Redford: Figure 1 element 18, column 2 lines 61-65)(Redford disclosed an SIMD processor. SIMD processors use the same functional unit to execute a single instruction with different data. The combination results in the functional unit and control unit of Masse being used for each of the four parallel functional units of Redford. This allows for operations to be repeated by a plurality of functional units.).

The advantage of SIMD processors is that they are able to efficiently processor arrays of data items (Redford: Column 1 lines 12-30). One of ordinary skill in the art would have been motivated by this advantage to implement SIMD onto the processor of Masse. Thus, it would have been obvious to one of ordinary skill in the art at the time of

the invention to implement SIMD processing on the processor of Masse for the advantage of efficiently processing arrays of data items.

11. As per claim 2:

Masse and Redford disclosed an apparatus according to claim 1, further comprising FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units (Masse: Figure 10 element 900, column 11 lines 1-33)(The memory that stores the repeat instruction is a FIFO because the repeat instruction that enters is the first repeat instruction to exit. Official notice is given that instructions can be stored in a register prior to execution. Thus, the memory storing the instruction in figure 10 is a register.).

12. As per claim 3:

Claim 3 essentially recites the same limitations of claim 5. Claim 3 additionally recites the following limitations:

wherein execution of the operations at the functional units is dependent at least in part on a state of the registers (Masse: Figure 10 element 922)(Execution is partly dependent on the loop counter register.).

13. As per claim 5:

Masse and Redford disclosed an apparatus according to claim 2, wherein said FIFO register means comprises a plurality of FIFO registers (Masse: Figure 10 element 900, column 11 lines 1-33)(The memory that stores the repeat instruction is a FIFO because the repeat instruction that enters is the first repeat instruction to exit. It's obvious to one of ordinary skill in the art that the memory can be expanded to store

additional repeat instructions that are within an executable program. In addition, according to *In re Rose*, 105 USPQ 237 (CCPA 1955), changes in size/range doesn't give patentability over prior art.).

14. As per claim 6:

Masse and Redford disclosed an apparatus according to claim 1, wherein each of said functional units are provided with at least one control unit (Redford: Figure 1 element 18, column 2 lines 61-65)(Redford disclosed an SIMD processor. SIMD processors use the same functional unit to execute a single instruction with different data. The combination results in the functional unit and control unit of Masse being used for each of the four parallel functional units of Redford. This allows for operations to be repeated by a plurality of functional units.).

15. As per claim 7:

Masse and Redford disclosed an apparatus according to claim 1, wherein the apparatus is adapted to form a pipeline consisting of a plurality of stages, wherein each stage is executed by a corresponding functional unit (Masse: Figure 5, column 6 lines 48-50)(The pipeline has a plurality of stages and each stage has a functional unit to perform the actions of each given pipeline stage.).

16. As per claim 8:

Masse and Redford disclosed an apparatus according to claim 1, therein for each control unit an instruction register (Masse: Figure 10 element 900, column 11 lines 1-33)(The memory that stores the repeat instruction is a FIFO because the repeat instruction that enters is the first repeat instruction to exit. Official notice is given that

instructions can be stored in a register prior to execution. Thus, the memory storing the instruction in figure 10 is a register.) and a counter are provided, wherein said counter indicates a number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit (Masse: Figure 10 element 922, column 11 lines 23-33)(The counter indicates the number of times instructions in the loop buffer are executed.).

17. As per claim 9:

Masse and Redford disclosed an apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units (Official notice is given that processors have both main memory and a hard disk memory, both of which store programs. Thus, it's obvious to one of ordinary skill in the art that the processor of Masse has both a main memory and a hard disk memory to store a main program that is being processed currently by the processor. Instructions stored in these memories inherently contain opcodes that will tell the control units how to perform the given instruction in the processor.).

18. As per claim 10:

The additional limitation(s) of claim 10 basically recite the additional limitation(s) of claim 1. Therefore, claim 10 is rejected for the same reason(s) as claim 1.

19. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 2. Therefore, claim 11 is rejected for the same reason(s) as claim 2.

20. As per claim 13:

The additional limitation(s) of claim 13 basically recite the additional limitation(s) of claim 7. Therefore, claim 13 is rejected for the same reason(s) as claim 7. Examiner also notes that each of the stages is executed by a functional unit, e.g., the fetch unit is a functional unit because it's function is performing instruction fetches.

21. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 8. Therefore, claim 14 is rejected for the same reason(s) as claim 8.

22. As per claim 16:

Claim 16 essentially recites the same limitations of claim 1. Claim 16 additionally recites the following limitations:

a fetch unit that is configured to retrieve instructions from a memory (Masse: Figure 5 element 204, column 6 lines 48-67 continued to column 7 lines 1-7); and

a decode unit that is configured to process the instructions to provide a plurality of sets of operations (Masse: Figure 5 element 206, column 6 lines 48-67 continued to column 7 lines 1-7),

wherein the fetch unit is configured to initiate execution of each set of operations at each corresponding functional unit for a given number of iterations (Masse: Figure 5 element 204, column 6 lines 48-67 continued to column 7 lines 1-7 and column 10 lines 1-18)(Fetching a CSR instruction initiates execution of the repeat instruction for a given number of iterations according to the instruction.)

23. As per claim 17:

Masse and Redford disclosed the processor of claim 16, wherein the sets of operations are configured to selectively include no-operation (nop) elements that facilitate synchronization among the functional units (Official notice is given that SIMD operations can be executed as no-ops. Thus, it's obvious to one of ordinary skill in the art at the time of the invention that SIMD operations can be executed as no-ops.).

24. As per claim 18:

The additional limitation(s) of claim 18 basically recite the additional limitation(s) of claim 3. Therefore, claim 18 is rejected for the same reason(s) as claim 3.

25. As per claim 19:

The additional limitation(s) of claim 19 basically recite the additional limitation(s) of claim 3. Therefore, claim 19 is rejected for the same reason(s) as claim 3.

26. As per claim 20:

Masse and Redford disclosed the processor of claim 16, wherein access to the memory for storing a result of the execution of the set of operations is limited to fewer than all of the functional units (Masse: Figure 10 element 908)(The execution results write their data to the register file. It's obvious to one of ordinary skill in the art that the results can be written out to a data cache by a store instruction.).

27. As per claim 21:

The additional limitation(s) of claim 21 basically recite the additional limitation(s) of claims 5 and 8. Therefore, claim 21 is rejected for the same reason(s) as claims 5 and 8.

28. As per claim 22:

Masse and Redford disclosed the processor of claim 16, wherein each local control unit signals the fetch unit upon execution of the set of operations in the register for the given number of iterations (Masse: Figure 10 element 932)(A repeat instruction can be repeatedly executed any number of times, including from a couple to hundreds of times. It's obvious to one of ordinary skill in the art that for a repeat instruction that executes hundreds of times, it would be beneficial to turn instruction fetching off until the repeat instruction is done executing. Thus, it's obvious to one of ordinary skill in the art that the control instruction would communicate with the fetching logic to save power by turning it off while long repeat instructions are executed.).

29. As per claim 23:

Claim 23 essentially recites the same limitations of claim 1. Claim 23 additionally recites the following limitations:

data transferred between the functional units is stored in a plurality of registers, states of the registers being dependent upon whether data is stored or retrieved from the registers (Masse: Figure 10 element 908)(Executed data by the functional units is stored in the registers. The state of a register can be controller by control signals during register read and write states of a processor pipeline.), and

synchronization among the functional units is controlled at least in part by the states of the plurality of registers (Masse: Figure 10 element 908)(The state of a register can be controller by control signals during register read and write states of a processor pipeline. Clock signals inherently control the timing of such reads and writes, which synchronizes the processor.).

30. As per claim 24:

Masse and Redford disclosed the processor of claim 23, wherein the plurality of registers includes one or more first-in/first-out registers, and the state of the first-in/first-out register is dependent upon whether the first-in/first-out register contains data (Masse: Figure 10 element 908)(The registers can be considered FIFO registers because data into a given register is the first data to be output of that register.).

Response to Arguments

31. The arguments presented by Applicant in the response, received on 4/9/2009 are not considered persuasive.

32. Applicant argues "Although Redford discloses a plurality of parallel datapaths for executing a single instruction, Redford does not disclose a plurality of control units. In the Office Action, page13, the Office argued that an SIMD instruction inherently has a plurality of execution units. However, it does not imply or suggest that each execution unit has its own control unit. Applicants submit that, as clearly shown in Fig. 1, Redford only discloses a single control logic 14, which sends the instruction to the datapaths 18 (column 3, lines 11 - 16). Furthermore, Redford (Figs. 2 and 4, column 3, lines 44- 56 and column 4, lines 38 - 52) discloses how the data items are assigned to the datapaths in each loop pass, and how to enable or disable each datapath" for claims 1, 3, and 10.

This argument is not found to be persuasive for the following reason. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on

combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Masse disclosed a single function unit that has its own local private control logic to control the execution unit by storing a counter value. The combination uses Redford to expand the functional unit of Masse into a plurality of functional units and control units to execute via an SIMD instruction. An SIMD instruction inherently has a plurality of execution units to execute the single instruction with different types of data. Thus, the combination multiplies the layout of figure 10 within Masse a plurality of times to correctly execute an SIMD operation. Thus, the combination reads upon the claimed limitation of each execution unit having a local control unit.

The examiner notes a possible amendment to overcome the rejections. Figure 3 appears to show that each functional unit is executing a specific task in a larger program. Thus, at any given point depending upon the instructions in a given task sent to the functional units, any number of functional units may be running a loop instruction. Therefore, the execution units can have zero, one, two, or three functional units running loop instructions concurrently. The combination of Masse and Redford only allows for all or none of the functional units to execute loop instructions at one point. Therefore, an amendment stating that a subset of the functional units running repeat/loop instructions in a clock cycle would overcome the rejection.

Conclusion

THIS ACTION IS MADE FINAL.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, Art Unit 2183